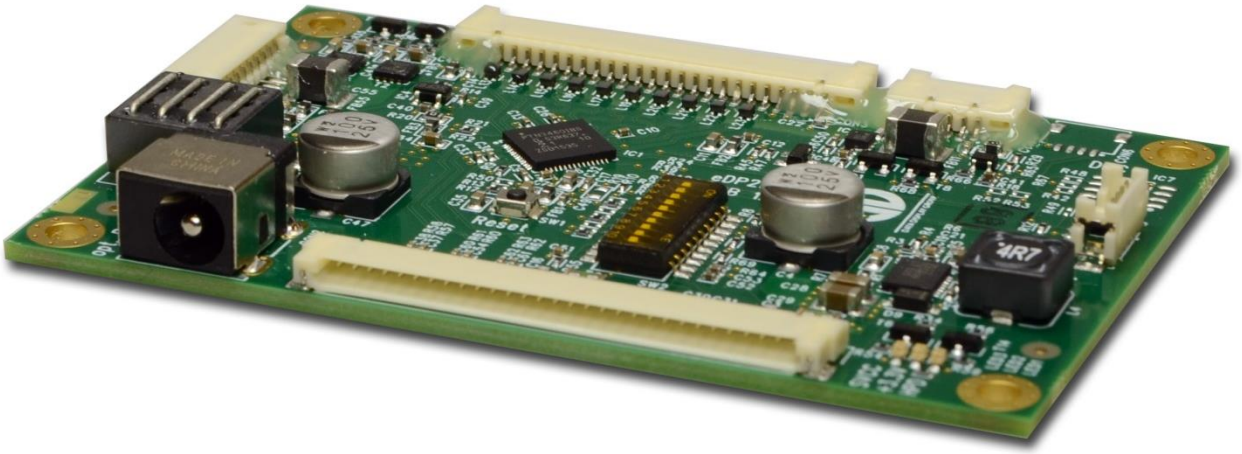
FORTEC
ELEKTRONIK AG

Datasheet

eDP2LVDS

eDP to LVDS Converter

ZU-09-031



Version 1.3

23.10.2018

Table of Contents

1 Revision History

Date	Rev.No.	Description	Page
19.11.2015	1.0	Initial version	All
25.04.2016	1.1	Release Version	All
08.08.2016	1.2	Add Note: BKL by AUX-channel on request.	15, 16
23.11.2018	1.3	Corrected LVDS output resolution Company logo updated Last page updated	4 All 18

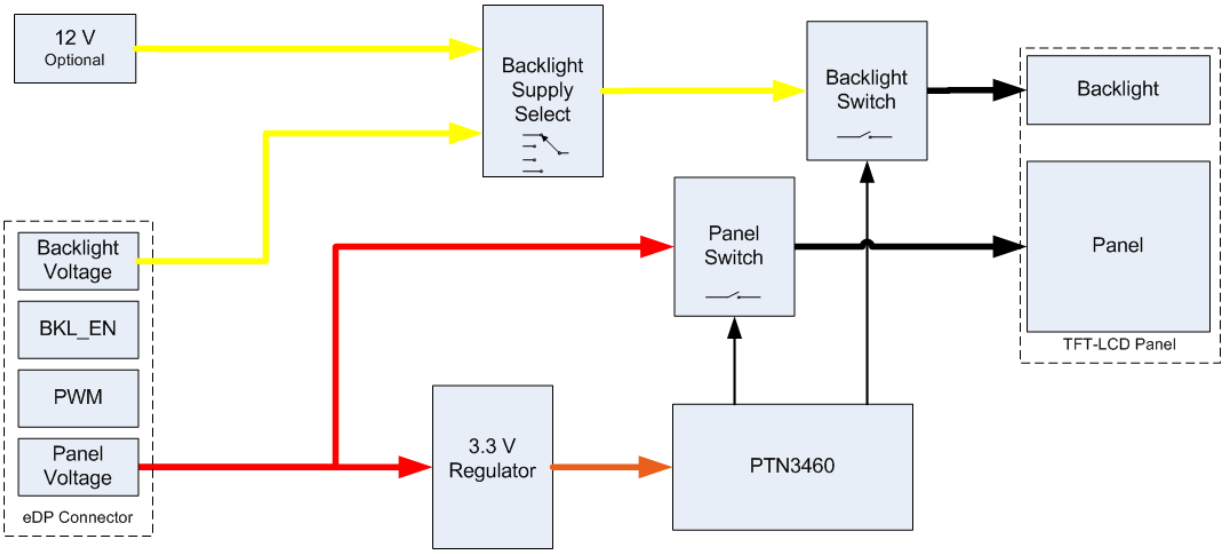
2 Overview

eDP2LVDS is a translator board which converts 1 or 2-lane eDP output to a single or dual channel LVDS connection. LVDS output connectors are Data Display Group company specific connectors which allow targeting a huge selection of panels.

3 Features

- Input: eDP – Embedded DisplayPort - eDP v1.2 and v1.1
  - 1 or 2 lanes (default mode is 2-lane operation)
  - Supports Reduced Bit Rate (1.62 Gbit/s) and High Bit Rate (2.7 Gbit/s)
  - eDP authentication options: Alternate Scrambler Seed Reset (ASSR) and Alternate Framing Output
  - supports Full Link training
- Output: LVDS
  - 1 or 2 Channels from 6 MHz to 112 MHz
  - Standard Data Display Group company specific output connectors Hirose DF14-25P
  - Supports 1920 × 1200 at 60 Hz resolution in dual LVDS bus mode
  - 18 Bit or 24 Bit output
  - VESA or JEIDA Mapping
  - Panel Power
    - pass-through from the eDP Input
  - Panel power up/down sequencing control
- Backlight
  - Pass-through or 12V external supply option
  - PWM Backlight dimming
    - Pass through or chip sequenced 3.3V
  - Backlight Enable Signal
    - Pass through or chip sequenced 3.3V
  - 24V Backlights supported with Prisma cables
- Power
  - Internal Logic is supplied from the Panel Voltage of the eDP Connector
  - Can be supplied from 3.3V to 12V with tolerances
- Additional Features
  - DIP Switch
  - EDID Emulation support
  - I2C Programming Connector

4 Power Concept



5 Absolute Maximum Ratings

Item	Symbol	Min.	Max.	Unit	Note
Supply Voltage	V_{in}	-0.2	16	VDC	1, 2, 5
Storage Temperature	T_{St}	-35	+85	°C	
Operating Temperature	T_{Op}	-25	+80	°C	3, 4

Note (1): Within operating temperature range.
Note (2): Permanent damage to the device or your display may occur if maximum values are exceeded.
Note (3): Specifications over the operating temperature range are assured by design, characterization and correlation with statistical process controls.
Note (4): Derating above 78°C, see sec. 5.2.
Note (5): This voltage is applied to panel without additional regulation. Please check your panel's specifications to not to damage your panel.

6 Electrical Specification

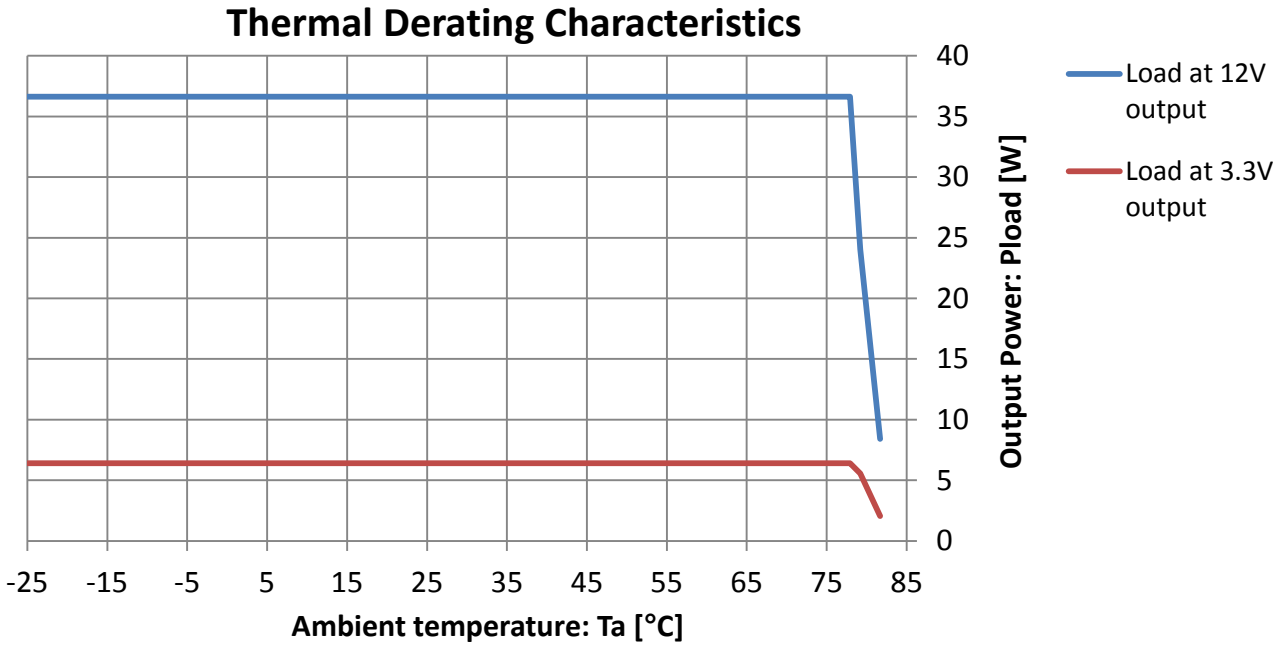
6.1 Operating conditions

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Supply Voltage	V_I	3	-	13	V	1
Backlight Voltage	V_{BKL}	10	12	15	V	1
Max Panel Current	$I_{PanelMax}$			2	A	
Max Backlight Current	I_{BklMax}			3	A	

Note (1): This voltage is applied to panel without additional regulation. Please check your panel's specifications to not to damage your panel.

6.2 Thermal Derating Characteristics

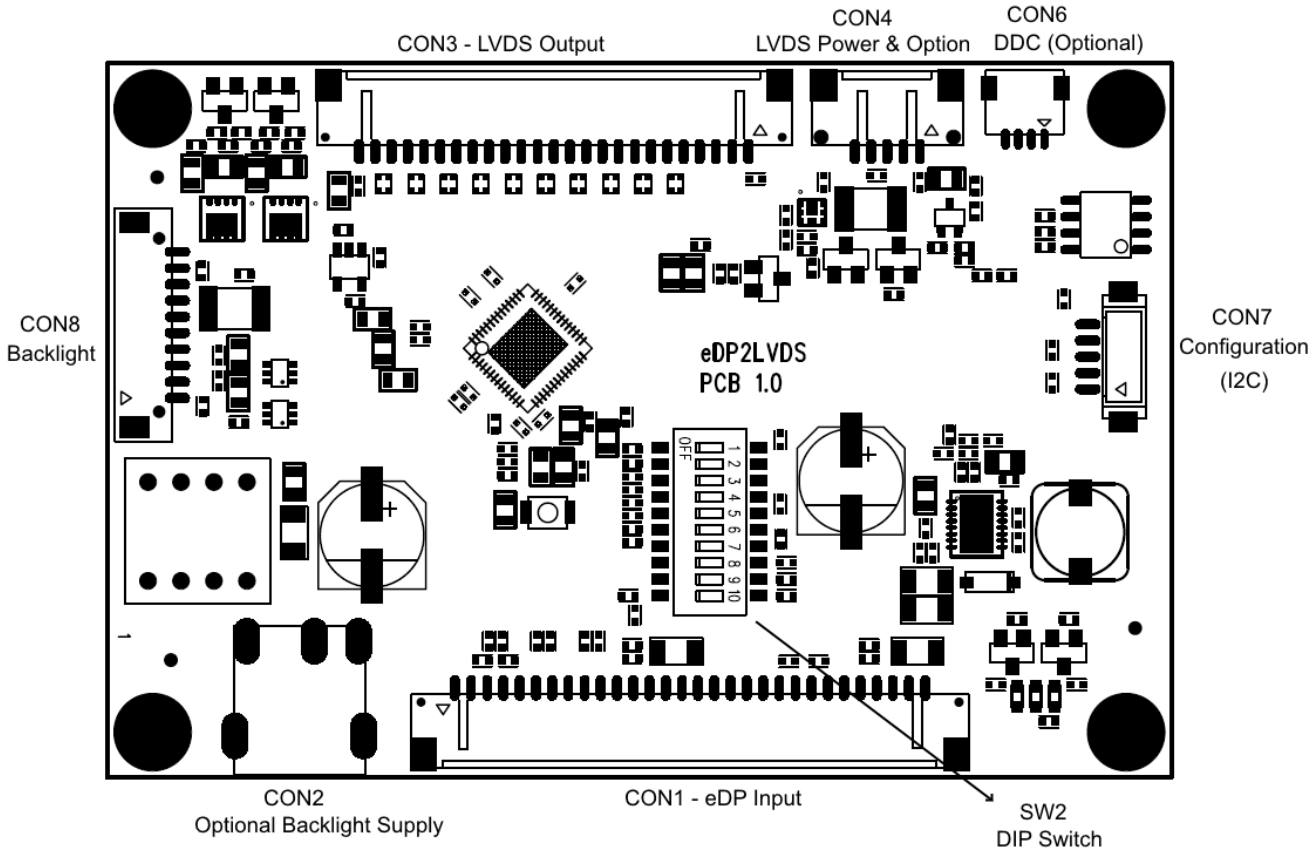
The following graph shows the external power consumption vs. temperature characteristics of the eDP2LVDS interface. The detailed limits for each output are described below.



Notes:

1) Within operating temperature range.
2) Permanent damage to the device may occur if maximum values are exceeded.
3) The 3,3V power consumption should not exceed 2W at the ambient temperature of 80°C. Additional, the power consumption should not exceed 6W at the ambient temperature of 78°C.
4) The 12V power consumption should not exceed 8W at the ambient temperature of 80°C. Additional, the power consumption should not exceed 36W at the ambient temperature of 78°C.

7 Connectors



Connector	Use	Manufacturer Part Number
CON1	eDP Input	Hirose DF14-30P-1.25H
CON2	Optional Backlight Supply	CUI PJ051AH
CON3	LVDS Output	Hirose DF14-25P-1.25H
CON4	LVDS Power & Option	Hirose DF14-5P-1.25H
CON6	Optional DDC Connection	Molex 501568-0407
CON7	Configuration (I2C)	Hirose DF13-5P-1.25V
CON8	Backlight	Hirose DF13-10P-1.25H

7.1 CON1 – eDP Input

eDP Input – CON1		
Pin	**Signal**	**Description**
1	--	Not Connected
2	GND	Ground
3	DPAUX_N	eDP Aux Channel -
4	DPAUX_P	eDP Aux Channel +
5	GND	Ground
6	DP0_P	eDP Channel 0 +
7	DP0_N	eDP Channel 0 -
8	GND	Ground
9	DP1_P	eDP Channel 1 +
10	DP1_N	eDP Channel 1 -
11	GND	Ground
12	SVCC_IN	Panel Power
13		
14	--	Not connected
15	GND	Ground
16		
17	HPD	Hot Plug Detect (HPD)
18	GND	Ground
19		
20		
21		
22	EDP_BKLT_EN	Backlight Enable – Input

23	EDP_PWM	Backlight Dimming - PWM Input
24	--	Not connected
25	--	Not connected
26	+12V_BKLT	+12V Backlight Supply Input
27		
28		
29		
30	--	Not connected

7.2 CON3 – LVDS Output

LVDS Output - CON3		
Pin	**Signal**	**Description**
1	SVCC_OUT	Panel power supply
2	SVCC_OUT	Panel power supply
3	GND	Ground
4	GND	Ground
5	TXA3+	LVDS data 1st pixel
6	TXA3-	LVDS data 1st pixel
7	TXACLK+	LVDS clock 1st pixel clock
8	TXACLK-	LVDS clock 1st pixel clock
9	TXA2+	LVDS data 1st pixel
10	TXA2-	LVDS data 1st pixel
11	TXA1+	LVDS data 1st pixel
12	TXA1-	LVDS data 1st pixel
13	TXA0+	LVDS data 1st pixel
14	TXA0-	LVDS data 1st pixel
15	TXB3+	LVDS data 2nd pixel
16	TXB3-	LVDS data 2nd pixel
17	TXBCLK+	LVDS data 2nd pixel clock
18	TXBCLK-	LVDS data 2nd pixel clock
19	TXB2+	LVDS data 2nd pixel
20	TXB2-	LVDS data 2nd pixel
21	TXB1+	LVDS data 2nd pixel
22	TXB1-	LVDS data 2nd pixel
23	TXB0+	LVDS data 2nd pixel
24	TXB0-	LVDS data 2nd pixel
25	BKLT_EN	Backlight Enable Signal

7.3 CON4 – LVDS Power & Option

LVDS Power & Option – CON4		
Pin	**Signal**	**Description**
1	LVDS_OPT_0	LVDS Option Signal
2	SVCC_OUT	Panel power supply
3	SVCC_OUT	Panel power supply
4	GND	Ground
5	GND	Ground

7.4 CON6 – Optional DDC Connection

Optional DDC Connection - CON3		
Pin	**Signal**	**Description**
1	DDC_SCL	DDC Clock
2	DDC_SDA	DDC Data
3	--	Not Connected
4	GND	Ground

7.5 CON7 – Programming Connector

Programming Connector – CON7		
Pin	**Signal**	**Description**
1	SDA	Serial Data / I2C
2	GND	Ground
3	+3.3V	+3.3V Supply Input
4	SCL	Serial Clock / I2C
5	--	Not Connected

7.6 CON8 – Backlight

Backlight – CON8		
Pin	**Signal**	**Description**
1	+12V_BKLT	Backlight Supply
2	GND	Ground
3	BKLT_EN	Backlight Enable
4	BRT_ADJ	Brightness Dimming
5	--	Not Connected
6	--	Not Connected
7	+12V_BKLT	Backlight Supply
8	+12V_BKLT	Backlight Supply
9	GND	Ground
10	GND	Ground

8 Customization – DIP Switch

Note: Reset the eDP2LVDS board after changing any of the DIP switch settings.

DIP Switch – SW2		
Bit	**Signal**	**Description**
1	BKLT_CTRL_BYPASS	Backlight Controls Selection
2	DUAL_LVDS	Single / Dual channel LVDS Selection
3	LVDS_MAPPING	LVDS Mapping Selection
4	LVDS_MAPPING	LVDS Mapping Selection
5	SINGLE_EDP	Single / Dual eDP Selection
6	EDID_EMU_OFF	Shutdown EDID Emulation / Activate DDC
7	LVDS_OPT_0	Change polarity of LVDS_OPT_0
8	BKLT_POWER_DELAY	Backlight Power ON Delay selection
9	BKLT_POWER_DELAY	Backlight Power ON Delay selection
10	BKLT_POWER_DELAY	Backlight Power ON Delay selection

Bit 1	**BKLT_CTRL_BYPASS**	**Note**
O	BKLT_EN and BRT_ADJ are controlled by PTN3460	1
X	Output signals BKLT_EN and BRT_ADJ are connected to input signals EDP_BKLT_EN and EDP_PWM and are controlled by external eDP source.	1

X= Switched ON **O**= Switched OFF

Note (1): The backlight control selection has great influence on the panel timing sequencing, which must comply with the panel specifications. Panel Power Sequencing is shown in Chapter 8.

Backlight Controls Selection: when this bit of the DIP Switch is switched OFF, BKLT_EN and brightness adjustment are controlled by PTN3460. In default state this bit is switched off. Please refer to Chapter 8 for more details.

Single / Dual channel LVDS Selection: Main chip PTN3460 is going to be configured for a single LVDS Output when this bit is switched on. eDP2LVDS board must be reset. In default state this bit is switched off.

LVDS Mapping Selection: This bit defines the mapping of the LVDS Output. Relation between switch bits and mapping is defined as follows. eDP2LVDS board must be reset. In default state these bits are switched off and LVDS is set to 24bpp – JEIDA Mapping.

Bit 3	Bit 4	LVDS Mapping
O	O	24 bpp – JEIDA (Conventional)
X	O	24 bpp – VESA (Nonconventional)
O	X	18 bpp
X	X	24 bpp – VESA (Nonconventional)

X= Switched ON **O**= Switched OFF

Single / Dual eDP Selection: Single lane eDP input can be enabled by switching on this bit. eDP2LVDS board. In default state this bit is switched OFF and eDP input is set to dual lane input.

Shutdown EDID Emulation / Activate DDC: In default state this bit is switched off and PTN3460 emulates the on-panel EDIDs of eDP panels. If the user's target LVDS panel has an EDID and the DDC channel of the panel is connected to CON6 then this bit can be switched on. In this case the LVDS panel's EDID is send to the source. Note that this is an assembly option, please contact your sales representative if you want to use this option.

Change polarity of LVDS_OPT_0: CON4 Pin1 is used as a general purpose configuration signal for LVDS Panels. Its polarity can be set using this bit. When this bit is switched on LVDS_OPT_0 signal will be logic high. It will be adjusted according to target panel.

Backlight Power ON Delay selection: Bit8, Bit9 and Bit10 define the delay between Panel power on and backlight power on. Default delay is 80ms.

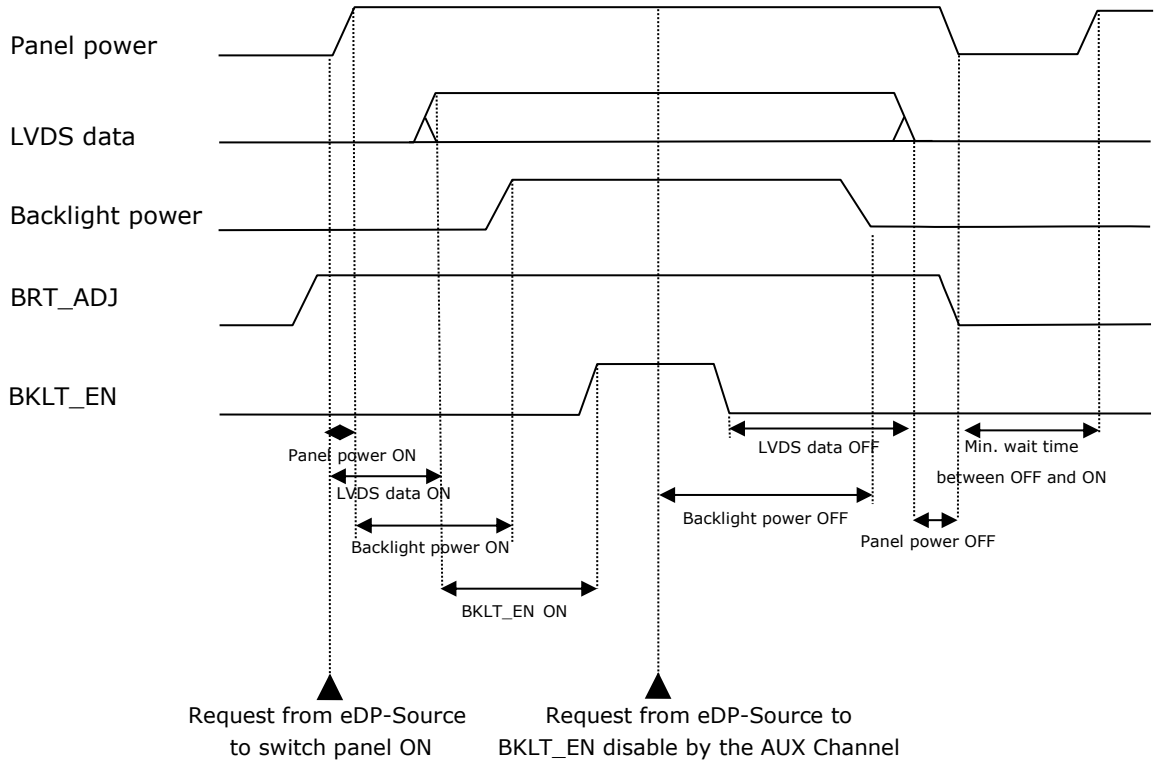
Bit 8	Bit 9	Bit 10	Delay
O	O	O	80 milliseconds
O	O	X	250 milliseconds
O	X	O	470 milliseconds
O	X	X	650 milliseconds
X	N	N	No delay

X= Switched ON **O**= Switched OFF **N**= Do not care

9 Panel Power Sequencing

DIP-Switch (Pin 1) is switched off

If the DIP-Switch (Pin 1) is switched off, BKLT_EN and BRT_AJD are controlled by PTN3460 chip. The BRT_AJD can be controlled by external eDP Source via AUX-Channel. Additionally, the shutdown process is influenced by the eDP-Source, this can turn off the Panel power or Backlight power prematurely. Please check the switch-off process at the eDP-Source and changed if necessary. Additional, please check your panel's specifications to not to damage your panel. The table below shows the programmable and adjustable hardware timings. During power-up, the BRT_ADJ value is set to a default value, see chapter 10.

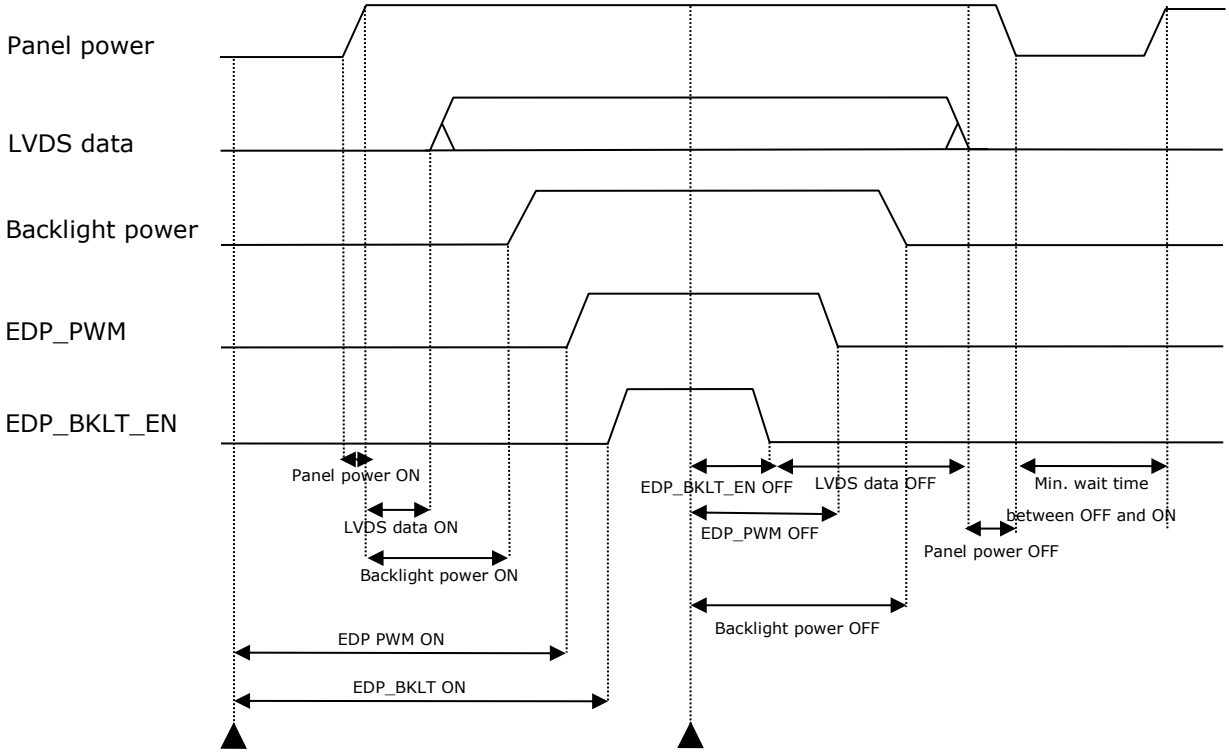


Item	Delay timing	adjustable via	Note
Panel power ON	5ms	--	(1)
LVDS data ON	16ms	I²C interface	(2)
Backlight power ON	0ms to 650ms	DIP Switch	(3)
BKLT_EN ON	> 200ms to 1000ms	I²C interface	(4)
BRT_ADJ ON	depending on the eDP-Source	AUX-Channel	(5)
BKLT_EN OFF	No delay	-	(6)
BRT_ADJ OFF	depending on the eDP-Source	AUX-Channel	(7)
LVDS data OFF	> 200ms to 1000ms	I²C interface	(8)
Backlight power OFF	depending on the source eDP	eDP-Source	(9)
Panel power OFF	16ms	I²C interface	(10)
Min. wait time between OFF and ON	> 500ms to 1000ms	I²C interface	(11)

Note (1): Fixed implementation in Hardware. Time interval between 10% and 90% of the Panel power.
Note (2): Time interval between Panel power ON signal and LVDS Data driven on LVDS interface. LVDS data ON is delayed by 16ms.
Note (3): DIP-Switch Bit 8, Bit 9 and Bit 10 define the delay between Panel power ON and Backlight power ON.
Note (4): The BKLT_EN On delay is the time interval between LVDS Data on and BKLT_EN rising edge on HIGH.
Note (5): The BRT_AJD signal must be controlled by the external eDP source via AUX channel. If the eDP source does not control this signal, BRT_AJD is switched on 410ms before the panel power (SVCC_OUT).
Note (6): The AUX channel sends the shutdown command for the BKLT_EN OFF signal. LVDS data OFF is the time interval between BKLT_EN signal made LOW and stopping of LVDS Data.
Note (7): The BRT_AJD falling edge on LOW must be controlled by external eDP source via AUX.
Note (8): The LVDS data OFF delay is the time interval between BKLT_EN falling edge on LOW and stopping of LVDS Data interface.
Note (9): Backlight power down sequence must be set at the eDP-Source.
Note (10): The panel power OFF is the time interval between LVDS data and panel power OFF.
Note (11): Time interval between Panel power switched off and panel power switched on.

DIP-Switch (Pin 1) is switched ON

If the DIP-Switch (Pin 1) is switched ON, the output signals BKLT_EN and BRT_ADJ are connected to input signals EDP_BKLT_EN and EDP_PWM and are controlled by external eDP source. Additionally, the shutdown process is influenced by the eDP-Source, this can turn off the Panel (SVCC_IN) or Backlight power (+12V_BKLT) prematurely. Please check the switch-off process at the eDP-Source and changed if necessary. The table below shows the still possible programmable and adjustable hardware timings. During power-up, the BRT_ADJ value is set to a default value, see chapter 10. BKL by AUX-channel on request.



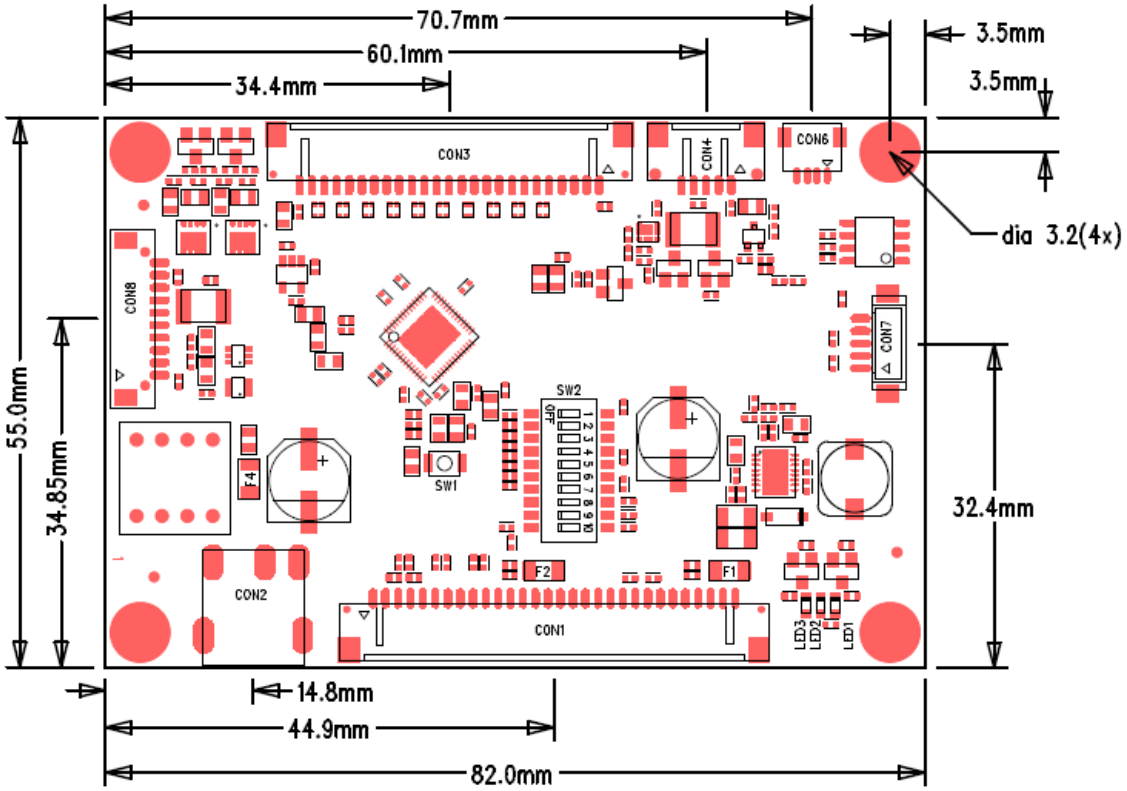
Request from eDP-Source to switch panel ON.

Request from eDP Source switches the EDP_BKLT_EN signal off it has to send an additional command via AUX channel to inform the PTN3460 about the start of the power down sequence. BKL by AUX channel on request.

Item	Delay timing	adjustable via	Note
Panel power ON	5ms	--	(1)
LVDS data ON	16ms	I²C interface	(2)
Backlight power ON	0ms to 650ms	DIP Switch	(3)
EDP_PWM ON	depending on the eDP-Source	eDP-Source	(4) (12)
EDP_BKLT_EN ON	depending on the eDP-Source	eDP-Source	(5) (12)
EDP_BKLT OFF	depending on the eDP-Source	eDP-Source	(6) (12)
LVDS data OFF	> 200ms to 1000ms	I²C interface	(7) (12)
EDP_PWM OFF	depending on the eDP-Source	eDP-Source	(8) (12)
Backlight power OFF	depending on the eDP-Source	eDP-Source	(9) (12)
Panel power OFF	16ms	I²C interface	(10)
Min. wait time between OFF and ON	> 500ms to 1000ms	I²C interface	(11)

Note (1): Fixed implementation in Hardware. Time interval between 10% and 90% of the Panel power.
Note (2): Time interval between Panel power ON signal and LVDS Data ON.
LVDS data ON is delayed by 16ms.
Note (3): DIP-Switch Bit8, Bit9 and Bit10 define the delay between Panel power ON and Backlight power ON.
Note (4): EDP_PWM ON delay must be set at the eDP-Source.
Note (5): EDP_BKLT ON delay must be set at the eDP-Source.
Note (6): When the eDP source switches the EDP_BKLT_EN signal OFF it has to send an additional command via AUX channel to inform the PTN3460 about the start of the power down sequence.
Note (7): The LVDS data OFF delay is the time interval between BKLT_EN falling edges on LOW and LVDS Data OFF.
Note (8): EDP_PWM OFF delay must be set at the eDP-Source.
Note (9): Backlight power down sequence must be set at the eDP-Source.
Note (10): The panel power OFF is the time interval between LVDS data and panel power OFF.
Note (11): Min. wait time between OFF and ON is the time interval between Panel power switched OFF and panel power switched ON.
Note (12): BKL by AUX-channel on request.

10 Mechanical Dimensions



11 Panel Power Sequencing configurations

Configuration	Panel	Presets	Note
DB-11-001	NL192108AC10-01D	LVDS data ON = 16ms	(1)
		Backlight power ON = 80ms	
		LVDS data OFF = 250ms	
		Panel power OFF = 16ms	
		Min. wait time between OFF and ON= 1000ms	
		BRT_ADJ value = 50%	

Note (1): DIP-Switch (PIN 1) is switched ON. Please refer to Chapter 8 for more details.

12 Application Notes

Please use the follow components for adaption a LVDS-TFT-Panel to an eDP signal source:

Configuration	eDP-Source	Panel	eDP Cable	LVDS Cable
DB-11-001	Intel NUC DE3815TYBE	NL192108AC10-01D	KA- 30-694	-
TBD	Intel NUC DE3815TYBE	G173HW01	KA- 30-694	KA-02 066-A

Our company network supports you worldwide with offices in Germany, Austria, Switzerland, Great Britain and the USA. For more information please contact:

Headquarters

Germany

FORTEC Elektronik AG
Lechwiesenstr. 9
86899 Landsberg am Lech

Phone: +49 8191 91172-0
E-Mail: sales@fortecag.de
Internet: www.fortecag.de

Fortec Group Members

Austria

FORTEC Elektronik AG
Office Vienna
Nuschinggasse 12
1230 Wien

Phone: +43 1 8673492-0
E-Mail: office@fortec.at
Internet: www.fortec.at

Germany

Distec GmbH
Augsburger Str. 2b
82110 Germering

Phone: +49 89 894363-0
E-Mail: info@distec.de
Internet: www.distec.de

Switzerland

ALTRAC AG
Bahnhofstraße 3
5436 Würenlos

Phone: +41 44 7446111
E-Mail: info@altrac.ch
Internet: www.altrac.ch

Great Britain

Display Technology Ltd.
5 The Oaks Business Village
Revenge Road, Lordswood
Chatham, Kent, ME5 8LF

Phone: +44 1634 672755
E-Mail: info@displaytechnology.co.uk
Internet: www. displaytechnology.co.uk

USA

Apollo Display Technologies, Corp.
87 Raynor Avenue,
Unit 1Ronkonkoma,
NY 11779

Phone: +1 631 5804360
E-Mail: info@apollodisplays.com
Internet: www.apollodisplays.com